REMARKS

Claims 1, 2, 4 and 7-19 are present in the present application, claims 3, 5 and 6 having been canceled, new claims 17-19 being added by this amendment. Reconsideration in view of the following remarks is kindly requested.

Entry of Amendment Requested

Applicants respectfully request entry of this amendment by the Examiner since it raises no new issues; and the claims as amended do not require any further consideration or search by the Examiner. Further, Applicants submit that, at the least, the amendment should be entered since it reduces the number of substantive and/or formal issues to place the application in better form for appeal.

Allowable Subject Matter

Applicants recognize and wish to thank the Examiner for the indication that claims 3, 5 and 6 are objected to as containing allowable subject matter, and would be allowable if rewritten into independent form including all of the limitations of the base claim and any intervening claims.

By this Amendment, Applicants have added new independent claims 17-19 that include the allowable subject matter of claims 3, 5 and 6 respectively.

Prior Art Rejections

The Examiner has rejected claims 1-2, 4, 7 and 9-16 under 35 U.S.C. § 102 as being anticipated by Applicants admitted prior art. This rejection is respectfully traversed.

Claims 1, 10, 13 and 15 have been amended to recite a data bus width conversion apparatus . . .the apparatus comprising, at least:

a setting section for **arbitrarily** setting the total number of transfer operations required for the first device to transfer the plurality of bit data groups, and for **arbitrarily** setting a division pattern of the N-bit data for dividing the N-bit data into the plurality of bit data groups, in combination with the other features or structural correlation recited in claims 1, 10, 13 and/or 15.

By **arbitrarily** setting the total number of transfer operations required for the first device and **arbitrarily** setting a division pattern of the N-bit data for dividing the N-bit

data into the plurality of bit data groups, the division pattern of data can be determined without hardware limitation as data read and write accesses are performed from a CPU (host) to a LSI (peripheral), see page 11, lines 2-14 of specification.

The AAPA states that the number of access operations by a CPU for transfer of N-bit data from the CPU to an LSI and the division pattern **are fixed in hardware so as to resize data bus width**. This makes it difficult to apply the conventional device to various bus systems (see page 2, lines 11-18 and page 4, lines 1-8 of specification).

Additionally, the Examiner has indicated that the prior art explicitly does not teach a setting section . . . having the advantage that the number of divisions and division pattern can be arbitrarily set (page 6, lines 9-11 of the final office action). Accordingly, for at least the above reasons, Applicants kindly submit that the Examiner withdraws the rejection and allow each of claims 1, 10, 13 and 15 and those claims dependent thereon.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of pending claims 1, 2, 4 and 7-19 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Matthew J. Lattig at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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